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PTO/SB/08A (08-00)
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U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>			Complete if Known		
			Application Number		
			Filing Date		
			First Named Inventor		
			Group Art Unit		
			Examiner Name		
			Attorney Docket Number		
Sheet	1	of	4	RBUS 1315-1	

U.S. PATENT DOCUMENTS						
Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
DmB	A1	4,384,354		Crawford et al.	05/17/1983	
	A2	5,122,978		Merrill	06/16/1992	
	A3	5,436,908		Fluker et al.	07/25/1995	
	A4	5,859,881		Ferraiolo et al.	01/12/1999	
	A5	6,047,346		Lau et al.	04/04/2000	
	A6	6,219,384		Kliza et al.	04/17/2001	
	A7	6,282,210		Rapport et al.	08/28/2001	
	A8	6,359,931		Perino et al.	03/19/2002	
	A9	6,396,329		Zerbe	05/28/2002	
	A10	6,442,644		Gustavson et al.	08/27/2002	
	A11	6,448,815		Talbot et al.	09/10/2002	
	A12	6,463,392		Nygaard et al.	10/08/2002	
	A13	6,469,555		Lau et al.	10/22/2002	
	A14	6,473,439		Zerbe et al.	10/29/2002	
	A15	6,510,503		Gillingham et al.	01/21/2003	
	A16	6,539,072		Donnelly et al.	03/25/2003	
	A17	6,556,934		Higashide	04/29/2003	
↓	A18	6,643,787		Zerbe et al.	11/04/2003	
DMB	A19	2003/0026399		Carlson	02/06/2003	
	A20					

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	B10							

Examiner Signature		Date Considered	6-21-05
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² Unique citation designation number. ³ See attached Kinds of U.S. Patent Documents. ⁴ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁵ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁶ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁷ Applicant is to place a check mark here if English language Translation is attached.

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DMB	A21	2001/0056332		Abrosimov et al.	12/27/2001	
DMB	A22	2002/0072870		Adam et al.	06/13/2002	
DMB	A23	2002/0138224		Sessions	09/26/2002	
DMB	A24	2002/0149824		Beaulieu et al.	10/17/2002	
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	B20							

Examiner Signature	<i>Dennis M. Butler</i>	Date Considered	<i>6-21-05</i>
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Filing Date		17 March 2004 (herewith)			
First Named Inventor		Scott C. Best			
Group Art Unit					
Examiner Name					
Attorney Docket Number		RBUS 1315-1			
Sheet	3	of	4		

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DmB	C1	PARIS, LLUIS ET AL, "WP 24.3 A 800MB/s 72Mb SLD RAM with Digitally-Calibrated DLL," IEEE International Solid-State Circuits Conference (1999), 13 pages.	
DmB	C2	NAKASE, YASUNOBU ET AL, "Source-Synchronization and Timing Vernier Techniques for 1.2-GB/s SLD RAM Interface," IEEE Journal of Solid-State Circuits, Vol. 34, No. 4 (Apr. 1999), 494-501.	
DmB	C3	GILLINGHAM, PETER, "SLDRAM Architectural and Functional Overview," SLD RAM Consortium (29 Aug 1997), 1-14.	
DmB	C4	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Draft 0.99 IEEE P1596.7-199X (1996), 56 pages	
DmB	C5	GILLINGHAM, PETER, "SLDRAM: High-Performance, Open-Standard Memory," IEEE (1997), 29-39	
DmB	C6	SLDRAM Inc., "400 Mb/s/pin SLD RAM," Draft Advance (9 Jul 1998), 1-69.	
DmB	C7	RAMBUS "Direct Rambus Short Channel Layout Guide, Version 0.95" (Aug	
DmB	C8	RAMBUS "Direct Rambus Long Channel Design Guide" (2000), 45 pages	
DmB	C9	RAMBUS, INC. "RDRAM Direct Rambus Clock Generator" (April 2002), 22	
DmB	C10	RDRAM® Overview, "High Performance Memory Interface Solution"; Copyright 2003 Rambus, Inc., all rights reserved, 4 pages	
DmB	C11	REDWOOD TECHNOLOGY BRIEF "High Performance Parallel Bus Interface Technology", Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	

Examiner Signature	<i>Dennis M. Butler</i>	Date Considered	6-21-05
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First Named Inventor		Scott C. Best			
Group Art Unit					
Examiner Name					
Attorney Docket Number		RBUS 1315-1			
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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DmB	C12	LEWIS, DAVE, "Easy-to-Use LVDS Serdes for the Serdes Neophyte" National Semiconductor, (16 June 2003), pp. 1-5.	
DmB	C13	INTEL "How to Measure RDRAM* System Clock Jitter" Application Note AP-667 (June 1999), pp. 1-15	
DmB	C14	U.S. Patent Application No. 10/278,748 filed 22 October 2002 entitled TIMING CALIBRATION APPARATUS AND METHOD FOR A MEMORY DEVICE SIGNALING SYSTEM, 186 PAGES.	

Examiner Signature	Dennis M. Butler	Date Considered	6-21-05
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Complete if Known

(Use as many sheets as necessary)

Application Number	10/802,634
Filing Date	17 March 2004
First Named Inventor	Scott C. Best
Art Unit	Unassigned
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1315-1

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6-21-05

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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		Application Number	10/802,634		
		Filing Date	17 March 2004		
		First Named Inventor	Scott C. Best		
		Art Unit	Unassigned		
		Examiner Name	Unassigned		
Sheet	2	of	2	Attorney Docket Number	RBUS 1315-1

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DMB	C1	Chang, Kun-Yung "Design of a CMOS Asymmetric Serial Link" A Dissertation Submitted to the Department of Electrical Engineering and the Committee on Graduate Studies of Stanford University August 1999, 119 pages	

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Complete If Known

Application Number	10/802,634
Filing Date	17 March 2004
First Named Inventor	Scott C. Best
Group Art Unit	2185
Examiner Name	Unassigned
Attorney Docket Number	RBUS 1315-1

Sheet 1 of 3

U.S. PATENT DOCUMENTS

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		Number	Kind Code ² (if known)			
DMB	A1	3,155,102		Niederer, Jr. et al.	11-03-1964	
	A2	3,638,121		Spilker, Jr.	01-25-1972	
	A3	3,922,491		Bjork et al.	11-25-1975	
	A4	4,648,133		Vilnrotter	03-03-1987	
	A5	5,243,626		Devon et al.	09-07-1993	
	A6	5,485,490		Leung et al.	01-16-1996	
	A7	5,511,091		Saito	04-23-1996	
	A8	5,523,760		McEwan	06-04-1996	
	A9	5,554,945		Lee et al.	09-10-1996	
	A10	5,621,913		Tuttle et al.	04-15-1997	
	A11	5,742,798		Goldrian	04-21-1998	
	A12	6,369,652		Nguyen et al.	04-09-2002	
	A13	6,421,389		Jett et al.	07-16-2002	
	A14	6,606,350		Dress, Jr. et al.	08-12-2003	
	A15	6,657,468		Best et al.	12-02-2003	
	A16	6,690,741		Larrick, Jr. et al.	02-10-2004	
	A17	6,717,992		Cowie et al.	04-06-2004	
	A18	2001/0048382		Low et al.	12-06-2001	
	A19	2001/0053175		Hector et al.	12-20-2001	
DMB	A20	2003/0026399		Carlson	02-06-2003	

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		Office ³	Number ⁴	Kind Code ⁵ (if known)				
DMB	B1	JP	02000035831A		Nitsusan Jidosha KK	08-14-1990	Abstract only	
	B2							
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Examiner
Signature

Dennis M. Butler

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	A22	2003/0146800		Dvorak	08-07-2003	
	A23	2003/0198212		Hector et al.	10-23-2003	
	A24	2003/0198308		Hector et al.	10-23-2003	
	A25	2004/0032354		Knobel et al.	02-19-2004	
↓ DmB	A26	2004/0057500		Balachandran et al.	03-25-2004	
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DMB	C1	ZERBE, JARED ET AL., U.S. Patent Application No. 09/776,550 filed 2 February 2001, entitled "Method and Apparatus for Evaluating and Calibrating a Signaling System."	
DMB	C2	ZERBE, JARED ET AL., U.S. Patent Application No. 09/976,170 filed 21 October 2001, entitled "Method and Apparatus for Evaluating and Optimizing a Signaling System."	
DMB	C3	U.S. Patent Application No. 10/278,708 filed 22 October 2002, entitled "Phase Adjustment Apparatus and Method for a Memory Device Signaling System."	
DMB	C4	DANIELE, N. et al., "Principle and Motivations of UWB Technology for High Data Rate WPAN Applications," SOC 2003, 4 pages.	
DMB	C5	WIN, MOE Z., et al., "Impulse Radio: How it Works," IEEE Communications Letters 2(2), Feb. 1998, 36-38.	
DMB	C6	DANIELE, NORBERT, "Ultra Wide Band Principles and Applications for Wireless Communications," CEA-LETI Annual Review, 25 and 26 June 2002, 24 pages.	
DMB	C7	U.S. Patent Application No. 09/941,079 filed 28 August 2001 entitled "Clock Data Recovery with Selectable Phase Control Input."	
DMB	C8	Yang, Chih-Kong Ken "Design of High-Speed Serial Links in CMOS" Technical Report No. CSL-TR-98-775, Sponsored By Center for Integrated Systems, Sun Microsystems and LSI Logic Inc. December 1998, pp. 1-182.	
DMB	C9	RaSer™ X Product Brief, "Highly Flexible 10 Gbps Backplane Serial Link Interface," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
DMB	C10	Yellowstone Technology Brief, "High Performance Memory Interface Technology," Copyright 2003 Rambus, Inc., all rights reserved, 2 pages.	
	C11		

Examiner Signature	Dennis M. Butler	Date Considered	6-21-05
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number 10/802,634
Filing Date 17 March 2004
First Named Inventor Scott C. Best
Group Art Unit 2115
Examiner Name Thomas C. Lee
Attorney Docket Number RBUS 1315-1

U.S. PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
DmB	A50	5,548,146		Kuroda et al.	08-20-1996	
DmB	A51	6,377,640		Trans	04-23-2002	
	A3					
	A4					
	A5					
	A6					
	A7					
	A8					
	A9					
	A10					
	A11					
	A12					
	A13					
	A14					
	A15					
	A16					
	A17					
	A18					
	A19					
	A20					

FOREIGN PATENT DOCUMENTS

Examiner Initials ¹	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
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	B10							

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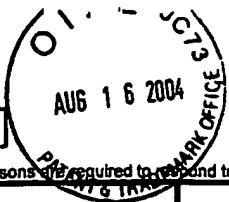
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Substitute for form 1449B/PTO		Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)		Application Number	10/802,634
		Filing Date	17 March 2004
		First Named Inventor	Scott C. Best
		Group Art Unit	2115
		Examiner Name	Thomas C. Lee
		Attorney Docket Number	RBUS 1315-1
Sheet	2	of	2

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
DMB	C27	WIDMER, A.X., et al., "A DC-Balanced, Partitioned-Block, 8B/10B Transmission Code," IBM J. Res. Develop., Vol. 27, No. 5, September 1983, 440-451.	
DMB	C28	BANU, MIHAI, et al., "TA 6.4: A 660Mv/s CMOS Clock Recovery Circuit with Instantaneous Locking for NRZ Data and Burst-Mode Transmission," IEEE International Solid State Circuits Conference, 1993, 102-103, 270.	
DMB	C29	ELDERING, CHARLES A., et al., "Digital Burst Mode Clock Recovery Technique for Fiber-Optic Systems," Journal of Lightwave Technology, Vol. 12, No. 2, February 1994, 271-279.	
DMB	C30	CHANG, KEN K. Y., et al., "A 2 Gb/s Asymmetric Serial Link for High-Bandwidth Packet Switches," Hot Interconnects V, Stanford University, August 1997, 1-9.	
DMB	C31	HU, TIMOTHY H., et al., "A Monolithic 480 Mb/s Parallel AGC/Decision/Clock-Recovery Circuit in 1.2-μ CMOS," IEEE Journal of Solid-State Circuits, Vol. 28, No. 12, December 1993, 1314-1320.	
DMB	C32	KIM, SUNGJOON, et al., "An 800Mbps Multi-Channel CMOS Serial Link with 3x Oversampling," IEEE 1995 Custom Integrated Circuits Conference, 22.7.1-22.7.4.	
DMB	C33	NAKAMURA, KAZUYUKI, et al., "A 6 Gbps CMOS Phase Detecting DEMUX Module Using Half-Frequency Clock," 1998 Symposium on VLSI Circuits Digest of Technical Papers, 196-197.	
DMB	C34	POULTON, JOHN, et al., "A Tracking Clock Recovery Receiver for 4Gb/s Signaling, Hot Interconnects '97, August 21-23, 1997, Palo Alto, CA, 1-13.	
DMB	C35	DALLY, W, et al., "DIGITAL SYSTEMS ENGINEERING," Cambridge University Press, 1998, pages 447-449.	
DMB	C36	CERISOLA, M., et al., "CORD - a WDM Optical Network: Control Mechanism Using Subcarrier Multiplexing and Novel Synchronization Solutions," Communications, 1995. ICC 95 Seattle, Gateway to Globalization, 1995 IEEE International Conference on , Volume: 1 , 18-22 June 1995 Pages:261 - 265 vol.1	

Examiner Signature	<i>Dennis M. Butler</i>	Date Considered	6-21-05
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